Digital Circuit Synthesis Using Universal Set of CMOS MVL Gates

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***Abstract*— The synthesis of digital circuits is generally performed in two level logic switching algebra. But if we increase the representation domain from two level logic (N=2) to N>2 then the design of Multiple Valued Logic (MVL) digital circuits is possible. Interconnections play an important role in deep sub-micron designs as they affects power and area. Due to the requirement of interconnections the design of binary logic is limited. In modern SoC designs,the interconnection is becoming a major problem which can be solved using MVL interconnection. Thus reduction in the area along with advantage of being able to easily interface with traditional binary logic circuits are the benefits of MVL digital circuits. A universal set of MVL CMOS gates can be used to synthesize and implement any MVL digital circuit. The lack of existing integrated circuits to implement the universal set of MVL gates is one of the major drawbacks. To overcome this issue, the design and implementation of a universal set of Integrated Circuits gates using CMOS 180nm technology is proposed which includes: Maximum (MAX), extended AND operators- eAND1, eAND2, eAND3, Successor (SUC) to synthesize any MVL circuit. The proposed gates allows designing of any MVL digital circuit by utilizing the knowledge coming from the binary circuits and extending it for the synthesis of MVL digital circuit.**

Keywords—Multiple valued logic, SoC

I. INTRODUCTION

Presently all the digital circuit synthesis is done in two level logic (L=2), where D = {0, 1} is the domain of numerical representation. Whereas if we increase the domain D = {0, 1, 2, …. K = L-1}, the synthesis of multi valued logic circuit is possible.MVL is also known as many valued or multiple valued or multi valued which traces its origin from the Post algebra and Lukasiewicz logic [1], [2].

Now a day, designers are facing new challenges due to the presence of large number of components in modern System on Chip (SoC). High integration of different systems on a single chip leads to an increment in the number and length of interconnections [3], the quantity and the delay time [4], and thus the overall complexity of the system is increased.

Therefore to overcome interconnection issue, multiple valued logics are proposed as they decrease the number of interconnections and processing components. By using MVL, the number of interconnections N can be reduced as inverse of $\log_2 N$. Thus reduction in area of integrated circuit occurs which promotes multi valued logic.

Also, MVL circuits can be used to represent numbers with fewer bits as compared to binary, e.g. the decimal number 255 is denoted as 11111111 in binary logic whereas 3333 in quaternary logic . Therefore since less no. of bits are required in quaternary logic, processing of the data become faster and also more reliable [5] [6] [7]. The possibility of representing the information using MVL is not recent. Flash memory has been successfully accomplished using MVL [8], for example, different logic values can be held by a single memory cell. Some combinational circuits like multipliers [9], adders [10], as well as FPGAs [11] were also proposed. These devices are based on current mode thus reducing area but due to the excessive power consumption & implementation complexities they are not suitable alternative for standard CMOS designs.

To overcome the issue of static power dissipation , a voltage mode MVL technique is presented in [12] by using a standard CMOS process and still maintaining low compaction by reducing the number of interconnections. Discrimination among the logic levels has to be done in voltage mode. To design the DLC (Down Literal Circuit) voltage discriminatory circuit Neuron MOS is used [13]. To define L logic levels with different threshold voltage, implementation of CMOS gates and PMOS and NMOS transistors is proposed in [14] and [15] respectively.MVL digital circuit synthesis comprised of operators and their properties. But the lack of existing IC that can implement universal set of gates and minimization tools for practical MVL circuit design serve as their main drawback

To overcome the first drawback ie lack of existing integrated circuit that can implement universal set of gates, design and implementation of universal set of IC gates based on 180nm technology is proposed in this paper. Universal set of IC gates for quaternary MVL algebra (where domain D = {0, 1, 2, 3}) comprised of five CMOS gates Maximum (MAX), Successor (SUC) and extended AND operators: eAND1, eAND2, eAND3.

Thus this paper presents design and implementation of universal set of MVL integrated circuit gates, initially

proposed in [16], in voltage mode utilizing CMOS technology and analysis of their transient response.

II. BASIC PRINCIPLES OF MVL

Depending on the assigned values to the inputs variables, MVL function will represent the value in domain D = {0, 1, …., K = L-1} and then a unique truth table can be obtained. Analogous to Products of Sums (POS) or Sum of Products (SOP) which is a unique representation of the function for binary algebra , canonical Sum of Extended Products (SOEP) form is defined for universal set of operators for quaternary MVL algebra. The already mentioned operators SUC, MAX, eAND1, eAND2, eAND3 in the introduction, define a universal set for quaternary logic under the proposed algebra.

Once the universal set is defined, to minimize the number of terms and literals of the MVL function postulates and theorems are needed, thus a minimal covering is determined. Also suitable algebra laws are defined to develop algorithms in a proper way and to implement software tools for performing the minimization. In binary algebra, there are many techniques for function minimization such as K maps, Espresso, Quine McCluskey etc [17]. Depending on the MVL algebra under consideration all these binary techniques can be extended to the MVL domain.

The next step for the synthesis is to design gates in either CMOS current mode or CMOS voltage mode. In voltage mode there is problem of how to define voltage levels to discriminate different logic reference levels for defining the threshold value of CMOS inverters. As this paper addresses voltage mode to design gate some characteristics must be defined to overcome this issue, for example - power consumption, frequency response, fan-in, fan-out, noise margins etc that has an effect on the W/L relation between the PMOS and NMOS gates and also on how to choose the reference voltage to discriminate among logic levels for the MVL. In recent years quaternary circuits has been studied increasingly as they have the practical advantage of transforming a four-valued signal into a two-valued signal.

The next step is to define an algebra which is easy to learn and convenient to use, must have a well-known methodology which is feasible to implement from both algorithmic and gates point of views. A possible way is to extend the well known concepts of the binary switching algebra to MVL algebra. This approach is adopted in this work.

III. MVL ALGEBRA: SUM OF EXTENDED PRODUCTS FORM:

MVL variables are denoted as $\mathbf{A_j}$ for notation purpose. MVL constants are represented by lower case letters such as j, k, l and the base of the digital representation is denoted by L with domain D = {0, 1, 2, …., K = L-1}. The Maximum operator is denoted by "+" symbol. The proposed closed MVL algebra is the ordered set with domain D in which acting one unary Successor(SUC) operator and two binary extended AND(eAND) and Maximum(MAX) operators (**+, *^{j}**) and two elements 0 and (L-1) with the following definitions.

Definition 1: Successor (SUC) operator is denoted by P^1 where P^1 = Q with Q being the next element after P^1 in cyclic ordered set D [18]. The notation P^1, P^2, P^3….. P^N indicates that the Successor operator is applied to P once, twice, thrice and so on upto N times. Note that $A_1{}^P = (A_1 + P)$ MOD L, where MOD stands for the modulo operator and symbol '+' stands for arithmetic addition here.

P	**P^1**	**P^2**	**P^3**
0	1	2	3
1	2	3	0
2	3	0	1
3	0	1	2

Table 1, Truth table for SUC operator

Definition 2: Extended AND (eAND) operator is denoted by $A_1 *^j A_2$ and by definition $A_1 *^j A_2 = j$ if $A_1 = A_2 = j$ else $A_1 *^j A_2 = 0$ as shown in Table 2 for quaternary logic D = {0, 1, 2, 3}.

A1/A2	**0**	**1**	**2**	**3**
0	0	0	0	0
1	0	1	0	0
2	0	0	0	0
3	0	0	0	0

A1/A2	**0**	**1**	**2**	**3**
0	0	0	0	0
1	0	0	0	0
2	0	0	1	0
3	0	0	0	0

A1/A2	**0**	**1**	**2**	**3**
0	0	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	1

Table 2, Truth table for eAND1, eAND2, eAND3 operator

Definition 3: Maximum operator is denoted by the symbol $A_1 + A_2$ and is defined as $A_1 + A_2 = A_1$ if $A_1 > A_2$ otherwise $A_1 + A_2 = A_2$.

A1/A2	0	1	2	3
0	0	1	2	3
1	1	1	2	3
2	2	2	2	3
3	3	3	3	3

Table 3, Truth table for MAX operator

Thus, these SUC, eAND and MAX operators form a universal set of gates [19], [20].

IV. IMPLEMENTATION OF MVL GATES:

1) SUGGESTED METHOD:

The IC implementation of universal set of gates is done to prove the concepts and feasibility of these gates to synthesis any discrete combinational and sequential circuit by utilizing the proposed algebra. Therefore instead optimization of IC, the main concern is MVL circuit design process and functionality. The methodology followed in this work is to first compare inputs with different threshold voltage threshold in order to identify four quaternary logic levels. Then the output of the comparator is fed to a set of control switches that set the output to four quaternary levels.

The design and implementation of universal set of MVL IC gates is divided into 3 circuit stages:

a) First stage has a 'discriminatory circuit' which identifies the input into four logic levels of quaternary domain (0, 1, 2, 3).
b) Second stage has a 'binary logic circuit' for performing binary logical operations to control set of switches.
c) Third stage has a 'set of switches' for setting the output voltage according to the output of second stage and to set the logic voltages in the output CMOS divider is designed.

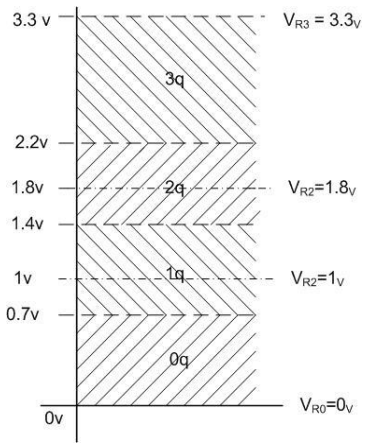

Fig. 1, Voltage values for Quaternary digit

For our experiments, 180nm CMOS technology is used. Generally binary logic values are represented by 0 V and 1 V that means the logic value '0' and '1' respectively. But in quaternary representation, four discrete voltage intervals are needed in order to represent four logic levels. Thus, the discrete voltage intervals 0 V- 0.7 V, 0.7 V-1.4 V, 1.4 V-2.2 V and 2.2V- 3.3 V are used to represent four quaternary logic levels '0', '1', '2' and '3' and these logic levels are denoted as 0_q, 1_q, 2_q, 3_q as shown in Fig. 1 and eq. (1). The threshold voltages 0.7 V, 1.4 V and 2.2 V in the vertical axis correspond with the V_{TH} shown in Fig. 2 shows standard inverter behaviour used as comparator in discriminatory circuit.

The implementation of circuit is done in partially binary circuit levels 0_b and 1_b with voltage levels of 0 V and 3.3 V, respectively.

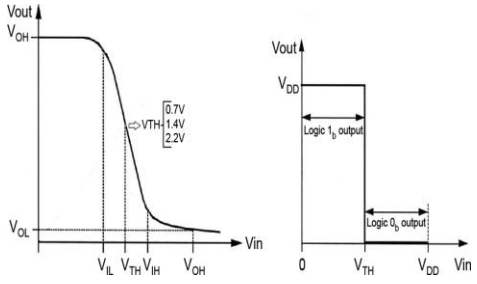

Fig. 2, Behaviour of Comparator

The output of the comparator is at 1_b level if the input voltage is less than V_{TH} represented as 3.3V in Fig. 2. Here the voltage level V_{dd} = 3.3 V represents both 1_b and 3_q. Thus, by comparing the input voltage against corresponding threshold, a unique quaternary digit (Q_{IN}) is set in the {0q, 1q, 2q, 3q} domain as follows:

$$QIN = f(VIN) = \begin{cases} 0q \text{ If } 0.0\ V \leq VIN \leq 0.7\ V \\ 1q \text{ If } 0.7\ V < VIN \leq 1.4\ V \\ 2q \text{ If } 1.4\ V < VIN \leq 2.2\ V \\ 3q \text{ If } 2.2\ V < VIN \leq 0.7\ V \end{cases} \quad -(1)$$

The transition voltages are determined by $(W/L)_P$ and $(W/L)_N$ of the PMOS and NMOS transistors in comparator. Table-1 shows (W, L) for PMOS and NMOS transistors for each inerter logic gate. Here for notation purpose INV_{07}, INV_{14} and INV_{22} are used to represent inverter logic gates with thresholds 0.7V, 1.4V, and 2.2V.

Inverter	Transistor	W	L
INV_{07}	NMOS	10µm	0.18µm
	PMOS	0.4µm	0.18µm
INV_{14}	NMOS	2.8µm	0.18µm
	PMOS	4.4µm	0.18µm
INV_{22}	NMOS	0.4µm	0.18µm
	PMOS	10 µm	0.18µm

Table 4, Width (W) and length (L) for Inverter Logic Gates

The value of the threshold voltage depends on W/L ratio. In Fig.1 the threshold voltage levels 0_q, 1_q, 2_q are evenly distributed except 3_q. Because in order put a value greater than threshold value V_{TH}= 2.2V, according to the simulation results the width of PMOS must be changed from W_p = 10µm to W_p = 60µm, which leads to unpractical design ($W_p \alpha V^4_{TH}$).

On comparing the input voltage VIN with different threshold voltages, the output of the inverters INV_{07}, INV_{14}, INV_{22} will be as follows:

If $V_{IN} > V_{TH}$ = 0.7 V, the output for inverter INV_{07} is 0_b, otherwise 1_b.

If $V_{IN} > V_{TH}$ = 1.4V, the output for inverter INV_{14} is 0_b, otherwise1_b.

Similarly, if $V_{IN} > V_{TH}$ = 2.2, the output for inverter INV_{22} is 0_b, otherwise1_b.

Now the value of unique quaternary digit (Q_{IN}) is set according to the output of inverters as follows:

If the output of INV_{07} is 1_b, then Q_{IN} will be 0_b.

If the output of INV_{07} and INV_{14} are 0_b and 1_b respectively, then Q_{IN} will be 1_q.

If the output of INV_{14} and INV_{22} are 0_b and 1_b respectively, then Q_{IN} will be 2_q.

If the output of INV_{22} is 0_b, then Q_{IN} will be 3_q.

2) MVL GATES:

a) SUCCESSOR (SUC) GATE:

Fig.3 shows the schematic of MVL SUC gate. It has one input and one output as shown in Fig. and output can have four possible values either 0_q or 1_q or 2_q or 3_q. To identify all the quaternary digits at input and then to set the output voltage as V_{R0} or V_{R1} or V_{R2} or V_{R3} , four switches MP0, MN0, MN1, MN2 and three inverters INV_{07}, INV_{14}, INV_{22} are used.

As shown in Fig.3, in order to define four reference voltages , gnd and V_{dd} = 3.3 V are used as two reference voltages V_{R0} and V_{R3} and a voltage divider circuit is used to establish the other two reference voltages ie V_{R1} and V_{R2}.

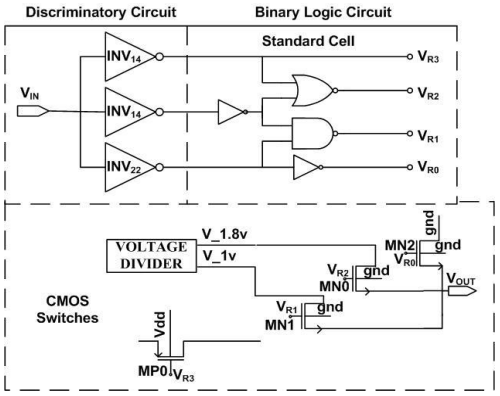

Fig. 3, Schematic of SUC gate

All the transistors MN0, MN1, MN2 and MP0 have one gate.

MN0, MN1, MN2 transistors has a length and width of 1µm whereas MP0has length of 1µm and width of 2.9µm.

b) EXTENDED AND1 (eAND1) GATE:

Fig.4 shows the schematic of eAND1 gate. It has two inputs (V_{IN1} and V_{IN2}) and one output (V_{OUT}). When both V_{IN1} = V_{IN2} = 1_q then only V_{OUT} = 1_q otherwise it will take value 0_q. Thus V_{OUT} can take two possible values either 0_q or 1_q.

The circuit will generate E or E_b signal when the first set of inverter INV_{07} and INV_{14} both will receive input1 ie V_{IN1} and the second set of inverter INV_{07} and INV_{14} both will receive input2 ie V_{IN2}. The two signals E and E_b will control a set of two switches MN0 and MN1 to set the output voltage as either V_{R0} = 0V ie 0_q or V_{R1} = 1V ie 1_q.

Where, E=NOT($V_{OUTINV07}$ OR NOT($V_{OUTINV14}$) OR $V_{OUTINV07}$ OR NOT($V_{OUTINV14}$)).

E_b = NOT(E).

Here, NOT denotes binary operator for Complement and OR denotes the usual binary operator OR.

As shown in Fig.4, in order to define four reference voltages , gnd and V_{dd} = 3.3 V are used as two reference voltages V_{R0} and V_{R3} and a voltage divider circuit is used to establish the other two reference voltages ie V_{R1} and V_{R2}.

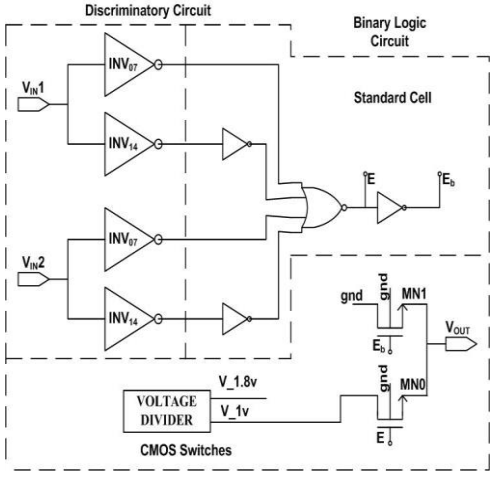

Fig.4, Schematic of eAND1 gate

Both the transistor MN0 and MN1 have one gate and has width equals to 2µm and length equals to 2µm.

c) EXTENDED AND2 (eAND2) GATE:

Fig.5 shows the schematic of eAND2 gate. Similar to eAND1, it also has two inputs (V_{IN1} and V_{IN2}) and one output (V_{OUT}). Here the set of inverter used in eAND2 consist of INV_{14} and INV_{22}.

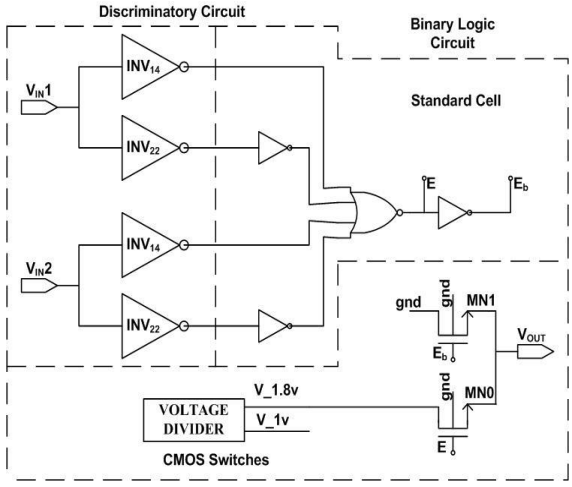

Fig.5, Schematic of eAND2 gate

d) EXTENDED AND3 (eAND3) GATE:

Fig.6 shows the schematic of eAND3 gate. The input voltages V_{IN1} and V_{IN2} are fed to two inverters INV_{22} and INV_{22}, respectively. The inverters will then identify the unique quaternary digit 3_q and the binary logic NOR gate will do the binary operations and internally it interconnects the output of the gate with the ref voltages either V_{R0} or V_{R3}. Since the value of the voltage for 0_q and 3_q are equivalent to 0_b and 1_b, respectively, this implementation is possible.

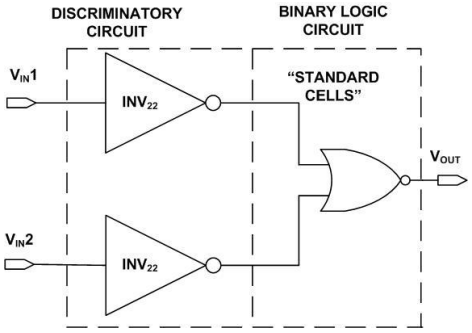

Fig.6, Schematic of eAND3 gate

e) MAXIMUM (MAX) GATE:

Fig.7 shows the schematic of MAX gate. It has two inputs (V_{IN1} and V_{IN2}) and one output (V_{OUT}) which can take any quaternary digit values (0_q, 1_q, 2_q or 3_q) according to the input. As shown in Fig.7, a voltage to current converter is used to convert input voltage signals into current signals and its output is fed to a current comparator in order to perform the comparison in current mode to determine the input having highest value. Then two switches MN1 and MP3 are used to connect the output to the highest input value which is controlled by the signals E and E_b.

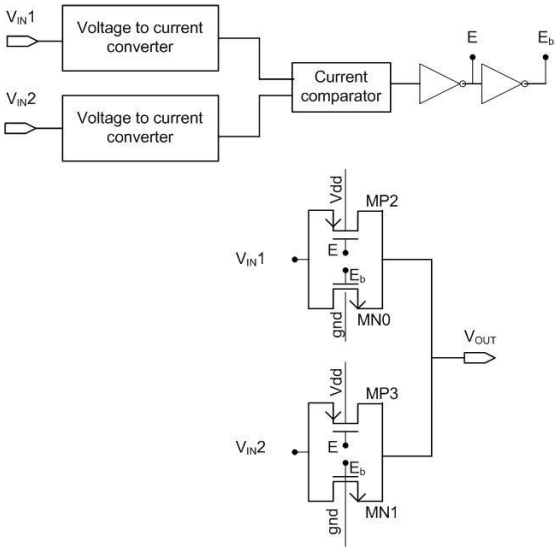

Fig.7, Schematic of MAX gate

V. SIMULATION RESULTS OF MVL GATES:

The simulation of proposed universal set of MVL gates is done using Cadance software. Fig. 8-12 shows the simulation results of universal set of gates (SUC, eAND1, eAND2, eAND3, MAX).

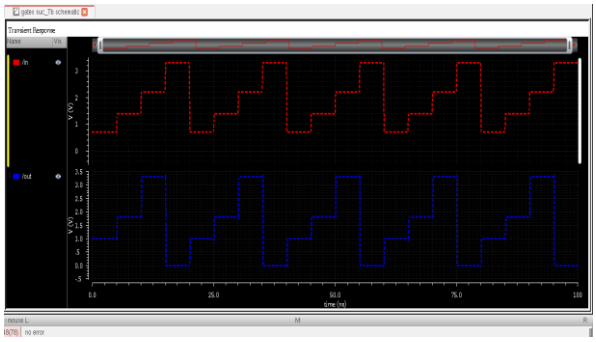

Fig.8, Transient response of SUC gate

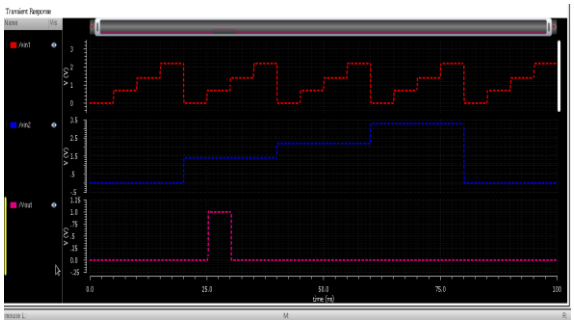

Fig.9 Transient response of eAND1 gate

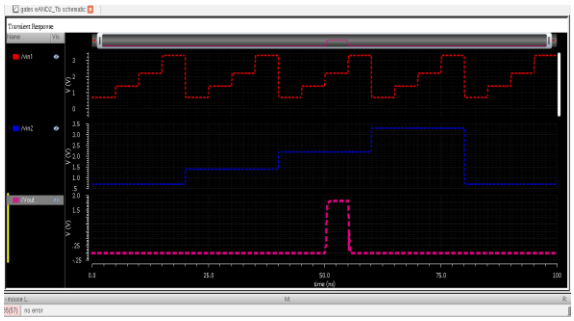

Fig.10, Transient response of eAND2 gate

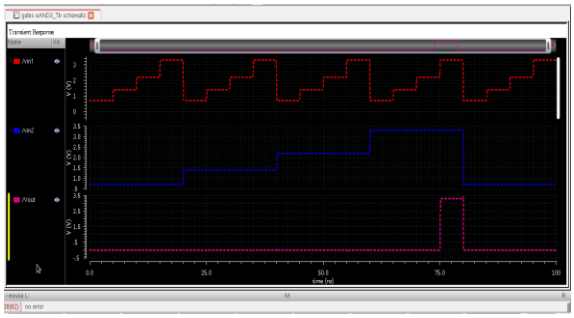

Fig.11, Transient response of eAND3 gate

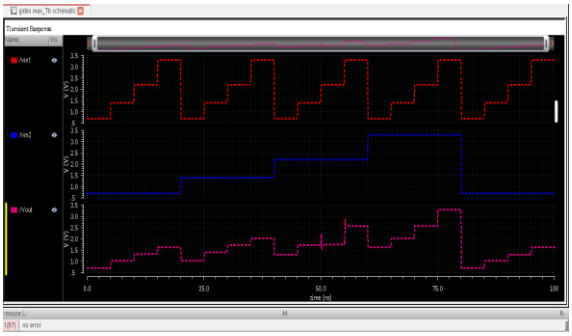

Fig.12, Transient response of MAX gate

For all the possible combination of input values it shows the corresponding output values or in other words shows the timing results for the proposed gates. Thus the correct functionality of the implemented universal set of MVL gates can be analysed by comparing the simulation results with the truth table shown in Table 1-3.

VI. CONCLUSION AND FUTURE WORK

In this paper an alternative method and algebra is proposed to design and synthesize multiple valued operators for designing digital circuit based on multi valued logic instead of binary logic. Five new gates SUC, eAND1, eAND2, eAND3 and MAX have been defined which can be used to design and implement any Multi Valued Logic digital circuit. The paper presented utilizes the knowledge coming from the binary logic digital circuit and extends it for the synthesis of digital circuit based on MV Logic. The results obtained by analysing the transient response of these MVL gates clearly shows the correct functionality of these multi valued logic gates and thus also shows the possibility of designing any sequential and combinational digital circuit based on multiple value concept. Future work will be done to show the implementation of these MVL based sequential and combinational circuit and also to improve the characteristics of these gates like fan in, fan out, delay etc.

REFERENCES

[1] J. Lukasiewicz, "On three valued-logic," in L. Borkowski, SelectWorks, Amsterdam, North-Holland, 1920, pp. 169–171.
[2] E. L. Post, "Introduction to a general theory of elementary propositions," Amer. J. Math., vol. 43, no. 3, pp. 163–185, Jul. 1921.
[3] C. Lazzari, P. Flores, and J. Monteiro, "Power and delay comparison of binary and quaternary arithmetic circuits," in Proc. 3rd Int. Conf. Signals, Circuits and Syst., 2009, pp. 1–6.
[4] C. Wu, Y. Li, and S. Chai, "Design and simulation of a torus structure and route algorithm for network on chip," in Proc. 7th Int. Conf. ASIC, 2007, pp. 1289–1292.
[5] Kenneth C. Smith, "Multiple-Valued Logic: A Tutorial and Appreciation," Computer, 21(4), 17-27 (1988).
[6] John T. Butler, "Multiple-valued Logic - Examining its Use in Ultrahigh Speed Computation," IEEE Potentials, 14(2), 11-15 (1995).

[7] M. Dornajafi, S. Watkins, B. Cooper, and M. Bales, "Performance of a quaternary logic design," in Proc. IEEE Region 5 Conf., 2008, pp. 1–6.
[8] Tae-Sung Jung, Young-Joon Choi, Kang-Deog Suh, Byung-Hoon Suh, Jin-Ki Kim, Young-Ho Lim, Yong-Nam Koh, Jong-Wook Park, Ki-JongLee, Jung-Hoon Park, Kee-Tae Park, Jhang-Rae Kim, Jeong-Hyong Yi, and Hyung-Kyu Lim. A 117-mm2 3.3-v only 128-mb multilevel NAND flash memory for mass storage applications. IEEE Journal of Solid-State Circuits, 31(11):1575–1583, Nov 1996.
[9] T. Hanyu and M. Kameyama. A 200 MHz pipelined multiplier using 1.5 v-supply multiple-valued mos current-mode circuits with dual-rail source-coupled logic. IEEE Journal of Solid-State Circuits, 30(11):1239–1245, Nov 1995.
[10] A.F. Gonzalez and P. Mazumder. Multiple-valued signed digit adder using negative differential resistance devices. IEEE Transactions on Computers, 47(9):947–959, Sep 1998.
[11] Z. Zilic and Z.G. Vranesic. Multiple-valued logic in FPGAs. Pages 1553–1556 vol.2, Aug 1993.
[12] R.C.G. da Silva, H. Boudinov, and L. Carro. A novel voltage-mode cmos quaternary logic design. IEEE Transactions on Electron Devices, 53(6):1480–1483, June 2006.
[13] S. J. Park, B. H. Yoon, K. S. Yoon, and H. S. Kim, "Design of quaternary logic gate using double pass-transistor logic with neuron MOS down literal circuit," in Proc. 34th Int. Symp. Multiple-Valued Logic, 2004, pp. 198–203.
[14] Y.Yasuda,Y. Tokuda, S. Zaima,K. Pak,T. Nakamura, and A. Yoshida, "Realization of quaternary logic circuits by n-channel MOS devices," IEEE J. Solid-State Circuits, vol. 21, no. 1, pp. 162–168, 1986.
[15] I. M. Thoidis, D. Soudris, and A. Thanailakis, "The design of low power multiple-valued logic encoder and decoder circuits," in Proc. 6th Int. Conf. Electronics, Circuits and Syst., 1999, pp. 1623–1626.
[16] M. E. R. Romero, E. M. Martins, and R. Santos, "Multiple valued logic algebra for the synthesis of digital circuits," in Proc. 39th IEEE Int. Symp. Multiple-Valued Logic, Los Alamitos, CA, USA, 2009, pp. 262–267.
[17] P. N. Victor, N. H. Troy, D. C. Bill, and J. I. David, Digital Logic Circuit Analysis and Design. Englewood Cliffs, NJ, USA: Prentice-Hall,2002.
[18] K. C. Smith. Multiple-Valued Logic: A Tutorial and Appreciation. IEEE Transactions on Computers, April 1988.
[19] H. H. Loomis Jr. and R. H. Wyman Jr. On Complete Sets of Logic Primitives. IEEE Transactions on Electronic Computers, EC-14(2):173–174, April 1965.
[20] P. Kerntopf, M. A. Perkowski, and M. H. A. Khan. On Universality of General Reversible Multiple-Valued Logic Gates. In Proceedings of the 34th International Multiple Valued Logic Symposium, pages 68–73, May 2004.